Inverter Architectures for active dv/dt filtering in WBG-based electric drives

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*Abstract*— Wide-bandgap (WBG) semiconductors are taking relevance in power electronics due to their superior electrical and thermal performance in comparison to conventional Si devices. While they are enabling various opportunities in the field of electric machines and drives, they produce a significant electric stress on the machine windings due their inherently elevated voltage gradients (dv/dt), resulting in a reduced lifetime of the entire system. A number of solutions are used nowadays to overcome such challenges, but their drawbacks do not always justify an effective implementation. In this paper, it will be proven how a suitable choice of the inverter can represent an effective, efficient and reliable means for active dv/dt filtering in electric drives equipped with WBG devices.

Keywords—SiC MOS, Reliability, Voltage Overshoot, dv/dt, PWM Inverter, PD, insulation degradation.

# Introduction

Power density and reliability have become the main objectives in the design process of electric drives and their components [1]. As higher speeds allow to achieve more compact machine designs, there has been a significant push towards the increase of switching frequencies of power converters, through the use of Wide-bandgap (WBG) semiconductors. Compared to conventional power electronics devices, WBG semiconductors feature better electrical and thermal properties [2]. Nevertheless, their high switching speeds produce also some drawbacks, due to inherently sharp voltage gradients (dv/dt) generated by the WBG-based converters. In turn, this could result in an excessive electric stress on the insulation system of the electric motor, thus reducing the overall reliability and lifetime [1],[3],[4]. More specifically, when steep rising and falling pulses occur, it is no longer possible to model the cables, connecting the electrical machine to the power converter, as a lumped parameters equivalent circuit. On the contrary, they act like transmission lines, with voltage waves travelling along the cables forward and backward. A constructive interference of these waves can lead to dangerous overvoltage at the motor’s terminals (almost twice the bus voltage), which may seriously affect the motor’s windings dielectric insulation [5].

In addition to this, the voltage distribution within the motor winding it is severely affected by the supply voltage waveform. In case of PWM converters, the voltage drop is unevenly distributed along the windings, with the majority of the voltage measured across the first windings’ turns. The phenomenon is more pronounced the higher is the dv/dt of the incident wave [6].

Thus, high voltage overshoots at the motor’s terminals and uneven turn-to-turn voltage distributions, may lead to excessive electric stress for the windings’ insulation system, resulting in premature aging or even in the triggering of disruptive Partial Discharge (PD) phenomena [7],[8].

Since this behaviour is exacerbated by fast devices’ commutations, the adoption of WBG devices, with very fast switching, poses serious interrogatives, which can prevent the full exploitation of this technology in real systems.

This is even more true in case of critical applications, such as aerospace, where the WBD devices represent a promising solution, but the Partial Discharge Inception Voltage (PDIV), namely the voltage level at which PDs start occurring, varies with the cruise conditions, as breakdown voltages decreases with the altitude according to Paschen's law. This may imply that drive systems, which are PD free at ground level, are no more at cruising altitude.

To deal with all these challenges, different design solutions can be identified at different drive levels. These include:

* Use of passive filters at the inverter output. This approach represents the most common solution adopted nowadays; with the insertion of RLC filters, a damping action is obtained on the voltage overshoot ensuring a smooth variation. The drawbacks of this solution are multiple: an increased complexity of the system, increased volume of the inverter, increased component count and thus reduced reliability, and increased power losses [9]-[11].
* Use of a new materials or thicker dielectric in the design of the windings’ insulation system [5]. One possibility is the adoption of a type II insulation system, classed as corona resistant, already used in high voltage machines [12]. This solution may however require the use of thicker insulating layers, reducing fill factor and thus the power density.
* Use of form-wound windings, i.e. hairpin conductors, in place of random-wound windings. This solution permits to clearly define the specific location of the conductors within the slots, thus reducing the electrical stress between adjacent conductors. Nevertheless, for this type of technology, a number of challenges needs to be addressed at high frequency operations, such as increased copper losses due to skin and proximity effects. However, innovative hairpin solutions, which minimize power losses at high frequency, have been proposed in [13] and [14], with promising result also for the aerospace sector
* Use of innovative design for the inverter. This solution, often referred as active dv/dt filtering, may involve the use of active gate drivers, which basically slow down commutation speed to maintain the voltage overshoot below a given threshold [15],[16]. This comes at the price of increased switching losses and a reduced efficiency of the converter but has the advantage to tailor the converter dv/dt to the specific application layout.

In alternative, multilevel converters and innovative inverter architectures has been proposed to minimize the voltage overshoot at the motor terminal maintaining the advantage of fast devices‘ commutations [17].

This paper is focused on this last solution. This aim of the work is to investigate innovative drive architectures with the ability to contain voltage overshoot at the machine terminals, minimizing the aforementioned detrimental effects of increased dv/dt, while maintaining the benefits deriving from the fast commutations of the devices.

To do so, several drive architectures already proposed in literature, along with a novel solution derived from some of the formers, are studied and compared. The analysis considers the behaviour of the different converters in a typical aerospace reference system and confronts the performance taking into account a number of figure of merits.

Unlike what is usually done, where converters are compared taking into account efficiency, complexity and perhaps cost and volume involved, in this work, for the first time, a comprehensive approach is adopted, in which the impact of converter operation on the lifetime of the driven motor is also considered. The aim it to favour the adoption of the best solution not only in terms of pure efficiency and cost, but instead of overall system reliability and performance.

The paper is structured in this way: in paragraph II the proposed architectures are presented with analytical computations for conduction and switching losses, in paragraph III comparisons on conduction and switching losses, reliability, overshoot voltage affection and costs are obtained, where in paragraph IVBOLOGNA

# Inverter Architectures: Description, conduction & switching losses

The analysed inverter structures, introduced in this section, are:

1. Two levels inverter (2-level),
2. Three levels Neutral Point Clamped NPC inverter (3-level),
3. Three levels T-type inverter (T-type),
4. Three levels inverter with voltage suppression (β-type),
5. Staggered multi-leg inverter (Multi-leg),
6. Multi-leg inverter with voltage suppression (proposed solution, PS).

The 2-level inverter, shown in Figure 1, is the simplest architecture and the one used as a benchmark in this work for the comparative study. As for all the other investigated architectures, only one leg instead of the full structure of the inverter is depicted, along with voltage waveform and driving signals. The output voltage waveform can be described as a step function passing from to (i.e. the DC-link voltage) and vice versa.

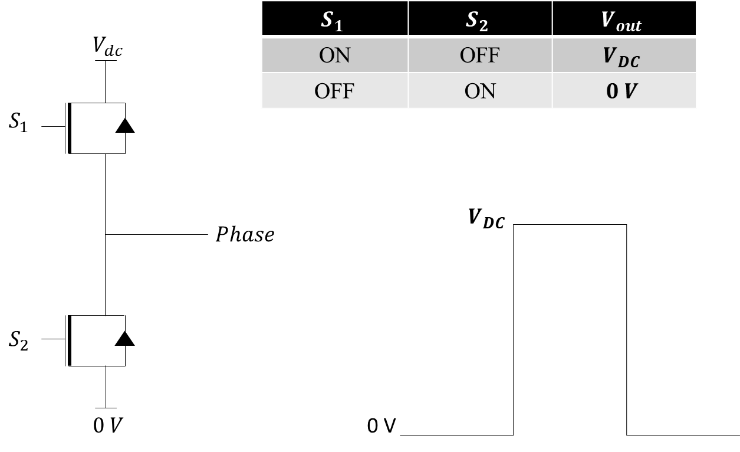


Figure 1 Single phase of the 2 level inverter

The 2 devices per phase switch in counter phase, i.e. when one is ON, the other is OFF and vice versa. Conduction power losses for 2 levels are computed in (1)

|  |  |
| --- | --- |
|  | (1) |

where with *RDSon* the equivalent on-state resistance of the MOSFET device, *i* the inverter output current flowing through the device and *D* its duty cycle. In case of variable frequency drive, *i*=*Im*\*sin(*ωt+θ*), with Im the peak of the inverter output current, ω its angular frequency, and θ the phase displacement between current and voltage.

In the 3-level inverter, shown in Figure 2, the clamping diodes and the two middle devices (S2, S3) force the output voltage to half of the DC-link voltage, obtaining a supplementary voltage level in addition to 0 and Vdc. During the positive half-wave, the output voltage switches between Vdc and Vdc/2, whereas commutation is between 0 and Vdc/2 during negative half-wave. This strategy has a number of advantages and devices half breakdown voltage than those used for the 2-level configuration can be adopted. The output voltage waveform guarantees reduced harmonic content and, more crucially, reduced dv/dt thanks to the smaller voltage difference in each step. Drawbacks include higher costs, conduction losses and complexity since the number of active devices is higher. For this solution, neutral point balancing is also required if a capacitor divider is used to generate the third voltage level [18]. conduction losses for external devices Pc\_ext are as in (2), whereas conduction losses for internal devices Pc\_int are reported in (3).

|  |  |
| --- | --- |
|  | (2) |
|  | (3) |

Diode conduction losses are in (4), where the voltage drop across the devices is expressed as with threshold voltage.

|  |  |
| --- | --- |
|  | (4) |

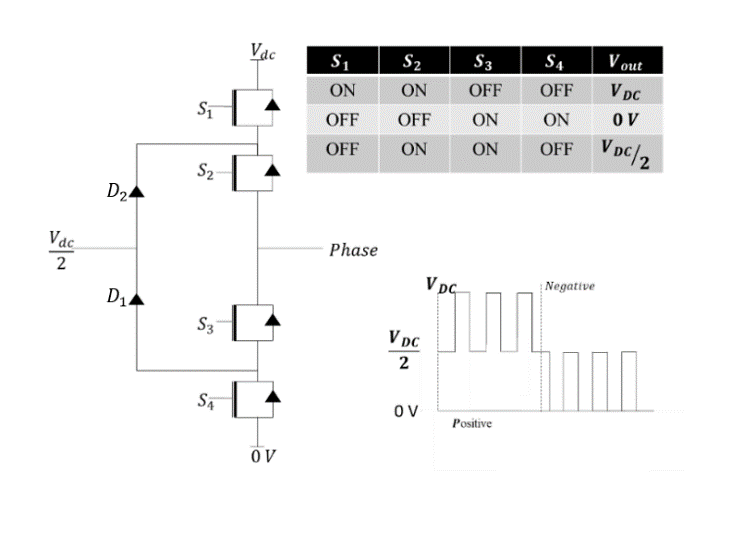


Figure 2 Single phase of 3-level inverter, positive and negative half period of output voltage wave

In the T-type inverter, whose circuital configuration is shown in Figure 3, the operating principle is the same as the one previously described, however, the exact details of how the clamping to half the DC link is performed differ between the two. In particular, the different transistor arrangement does away with the requirement for the two clamping diodes in favour of two devices in antiseries configuration (S3 and S4) [19]. The architecture has the potential of reducing conduction losses (depending on the type of transistor used) compared to 3-level NPC, thanks to the lower number of devices in conduction when converter is outputing 0 and Vdc voltages, however, the main devices (S1 and S2) need to block the whole dc link voltage, as with the two level converter.In a T-type architecture, conduction losses for external devices are the same as in (2), whereas Pc\_int can be computed as in (5).

|  |  |
| --- | --- |
|  | (5) |

## A picture containing graphical user interface Description automatically generated

Figure 3 Single phase of T-Type inverter, positive and negative half period of output voltage wave

The β-type topology is a hybrid between the common two level and the T-type architectures. Hardware wise, the device configuration is the same of the T-type inverter, allowing the output waveform to have three levels.

By contrast with the traditional 3-level architectures, this one uses the middle voltage level only for a very short time during the commutation event, in order to reduce the voltage gradients at the machine terminals [20].

This can be appreciated in Figure 4 where a short interval , during which the output voltage stays at Vdc/2, is interposed in each transition between 0 and Vdc of the inverter output voltage.

The basic idea is defined on reflection of the voltage waveform. Knowing the impedance of the cable, the delay experienced by the voltage waveform travelling from the inverter output to the electrical machines (EM) can be computed as seconds, where L and C are respectively the per meter inductance and capacitance of the cable. At motor terminal the wave is reflected back due to the mismatch between cable and motor input impedances. Thus, after 2τ, the voltage waveform returns at the inverter output with a phase delay of 2π. At this point, if a new voltage transition is generated, the two waves constructively interfere dumping the resonance. For this reasons, if almost no voltage overshoot takes place at the motor terminal.

The time spend in this middle voltage level need to be tailored considering the specific operational condition, but it is in general very small when compared with the whole switching period (i.e. only up to few hundred nanoseconds). This allows drastic simplification of the hardware design when compared to a traditional three level converter, as the third level does not carry any significant amount of current, mostly eliminating the need for neutral point balancing. In addition, the two transistor in position S3 can also be much smaller than the other ones, lowering cost significantly. All these considerations make it possible for this architecture to have a significantly different losses profile than conventional T-type converter. Conduction losses for Beta inverter are computed in (3):

|  |  |
| --- | --- |
|  | (6) |

## 

Figure 4 Single phase of Beta inverter

In Figure 5, the staggered switching inverter, referred as Multi-leg, is reported [21]. It is based on a number of independent two level legs, that are connected to the load through a binary tree of summing junctions, each one implemented as an interphase coupled inductor.

Depending on how many legs are on at the same time a different voltage level will be seen on the output. By turning on the legs sequentially in a staggered order, a multi-step waveform is created. The number of steps depends on the number of the legs considered. In the case described in Figure 5, with 4 legs involved, the voltage takes three different intermediate levels between 0 and Vdc, each maintained for a time , with τ the propagation time of the voltage wave.

Although this topology involves a higher number of devices, each conducts only a fraction of the output current, resulting in reduced conduction losses for a given MOSFET. Considering that current trough devices remains constant from seconds to seconds, it is possible to simply the computation of conduction losses in (7):

|  |  |
| --- | --- |
|  | (7) |

## 

Figure 5 Single phase of Multi-leg inverter

The last solution analysed is the multi-leg inverter with voltage suppression, reported in Figure 6. This proposed solution can be seen as a composition of the β-type and the multi-leg inverters.

This optimization allows the output waveform to have the same number of levels as in the previous topology, while at the same time reducing the depth of the output addition tree by one level, eliminating two combining coupled inductors, increasing both efficiency and power density with the same number of switching devices.

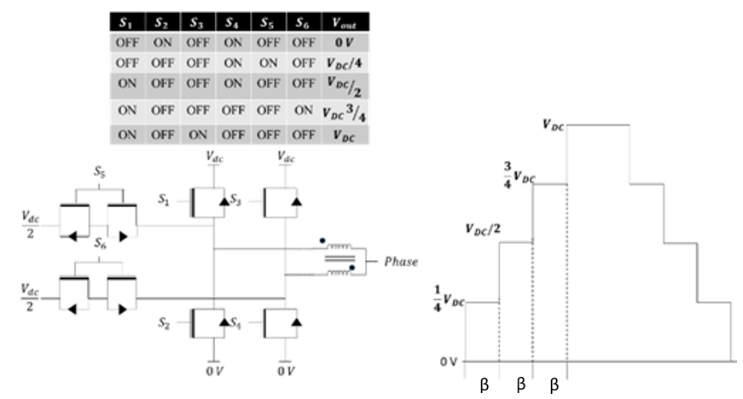


Figure 6 Single phase of the proposed solution

Same consideration as Multi-leg structure can be done for the proposed solution changing current value dividing the total current by 2 instead of 4 as in (7). Finally, conduction losses can be obtained in (8):

|  |  |
| --- | --- |
|  | (8) |

For switching losses, datasheets report energy losses during turn-on and turn-off considering specific test conditions for current and voltage, i.e. and . The energy losses due to reverse recovery of antiparallel diodes are usually embedded in the given figures. Thus, the equations that describe such loss contributors are reported in (9) and (10), where and Im are the actual voltage and current values at which the device turns on and off, is the switching frequency, is the turn-on energy loss, is the turn-off energy loss.

# Comparison of the analysed Architectures

## Reference system used for the comparison

The reference system chose for the analysis is a typical electrical actuator for aerospace applications driving an hydraulic circuit, e.g. for primary and secondary flight control surfaces actuation, landing gear extension/retraction

mechanisms etc. It consists into an inverter, which controls an electrical machine by means PWM voltage supplied via appropriate cabling (see Figure 7)

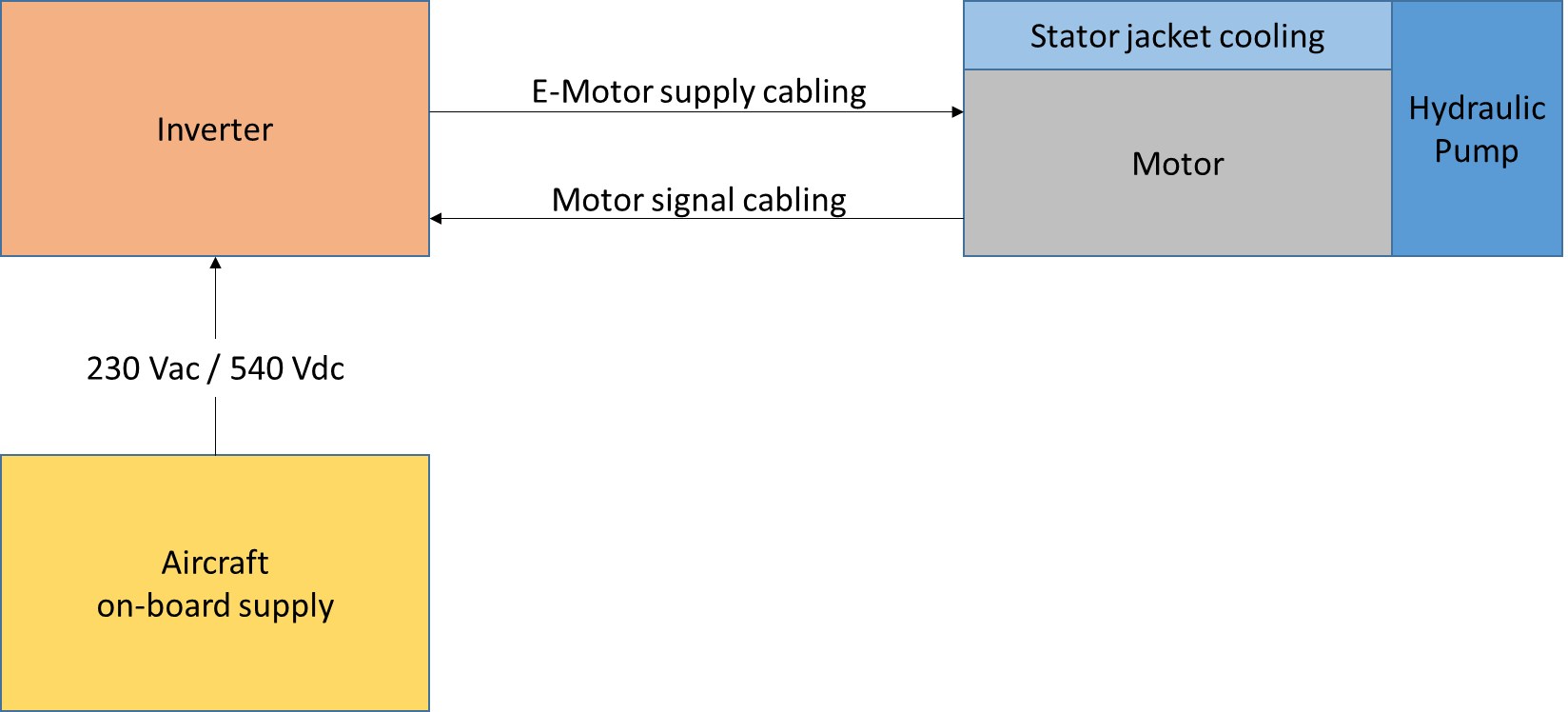
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Figure Reference sysetem structure

The inverter is directly connected to rectified A/C on-board voltage supply (typically 230Vac, 360-800Hz) [23]. The DC-link nominal voltage is 564 V. However, during system operation DC voltage is subject to variations up to 840 V due to normal or abnormal transient operations, as defined in RTCA DO-160 [24] and reported in Table 1.

The electrical machines is an IPM, random wound, distributed fractional lapped windings, which parameters are reported in Table 1 along with cable characteristics.

Target time over the complete life is 150000h in unpressurised environment.

In fact, actuators for the MEA have much different ambient operating conditions, with temperatures ranging from -55 °C to +70°C, with the latter the highest temperature the equipment will normally be exposed to and expected to operate. Figure 8 shows the joint probability density (JPDF) of the atmospheric conditions encountered by a commercial plane.

The JPDF was estimated using the IAGOS database using all available data for the year 2015 [25]. Commercial aircrafts spend most of the time at altitudes where the pressure is about 20 kPa (200 mbar) and temperatures from -60°C and -40°C. This represents a challenge for power electronics system and the insulation system of the electrical machines in particular, as PDIV strongly lowers when pressure decreases.

The analysis considers a short duty application. In these drives, the EM is required to deliver a high level of torque in a relatively short amount of time, which is generally below ten minutes.

In the following the inverter architectures are compared in terms of power efficiency, reliability of the inverter structure (considering as primary fault cracks in the aluminium bond wires of the power modules due to thermal cycling), level of induced electrical stress on the machine’s insulation system leading to windings’ degradation and overall cost considerations.

Table Reference System parameters

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter name** | **Value** | | |
| **Electrical Machine** | | | |
| Nominal Torque  Rotational speed  Power  Max operational current  Pole pairs | 21,3 Nm  Nominal 2600 rpm – Max 9000 rpm  Min op. 3,87 kW – Max op. 13,68 kW  Min op. 44.6 Arms – Max op. 50.91 Arms  4 | | |
| **Cable** | | | |
| Length  Resistance  Capacitance  Inductance | 6 m  2.27 mΩ/m  55.27 pF/m  368.70 nH/m | | |
| **Inverter** | | | |
| DC Link voltage | Voltage (V) | Percentage of System Time (%) | Operation ref. RTCA DO-160 |
| 564 | 79.6 |  |
| 620 | 19.9 |  |
| 692 | 0.27 | abnormal transient |
| 795 | 0.08 | normal transient |
| 842 | 0.03 | abnormal transient |
| Switching frequency | 20 kHz | | |



Figure 8 Single phase of the proposed solution

## Efficiency Comparison

To perform the comparative analysis among all the investigated inverter architectures, two types of Silicon Carbide (SiC) MOSFETs are used. The first type is a Littelfuse LSIC1MO120E0080, a 1200V class MOSFET (80 mΩ nominal RDSon) that is used where the entire DC-link voltage must be blocked by a single device. The second one is Infineon IMW65R048M1H that can hold only up to 650V (48 mΩ nominal RDSon). This choice has been made not to artificially cripple the performances of architectures, such as the diode clamped NPC (3-level), where two devices are used in series but must withstand half of DC-link voltage.

The two devices have similar characteristics in term of continuous drain current: 39 A @ 25 °C and 25-24 A @ 100 °C of case temperature TC. Considering maximum operational currents in Table 1, each switching block, generally schematized as single devices in Figure 1 to Figure 4, should be composed by at least three of these devices in parallel to safely deliver the required current at max TC. This consideration is not valid for block S3 of β-type topology, which power losses are very limited and even devices with lower rated current could be adopted in an optimized solution.

However, as Multi-leg and Proposed solutions present a different devices’ distribution compared to these other architectures, a choice of four devices in parallel for each switching block had been made to perform a fare comparison.

For the sake of completeness, in Table 2 the number of SiC MOSFET utilized in all the topologies is summarized with in red the number of parallel devices. Note that for the 3-level inverter, the body diode of IMW65R048M1H is employed for the half DC-link clamping diodes.

A thermal analysis was performed in PLECs imposing for all the architectures the simulation parameters in Table 3.

Two different switching frequencies have been analysed, the nominal 20 kHz of the reference system and its double, 40 kHz, to investigate the possibility of exploiting more SiC fast commutation performance.

*Table 2 Number of devices per architecture*

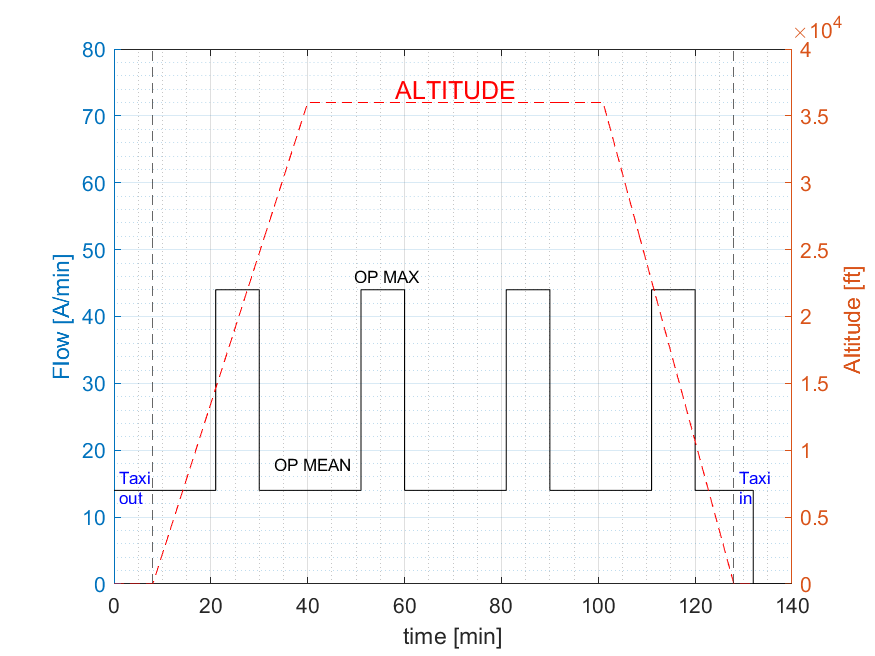
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| --- | --- | --- | --- | --- | --- | --- |
| MOSFET | 2-level | Beta-type | 3-level | T-type | Multi-leg | PS |
| 650V IMW65R048M1H | 0 | 6 | 12x4+6x4 diodes | 6x4 | 0 | 12 |
| 1200V LSIC1MO120E0080 | 6x4 | 6x4 | 0 | 6x4 | 24 | 12x2 |
| Coupled Inductors | 0 | 0 | 0 | 0 | 18 | 6 |

Table Simulation Parameters

|  |  |
| --- | --- |
| DC Link voltage VDC | 500 – 800 V |
| Output Current I | 5-20 A |
| Switching frequency fSW | 20-40 kHz |
| Fundamental frequency of the modulated voltage fC | 50 Hz |
| Load Resistor Rload | 1.9 Ω |
| Load inductor Lload | 1 H |
| Series resistance for coupled inductors RCI | 1 m |

## Working cycle description

The working cycle of the hybrid system for this aerospace application duration is 132 minutes divided in 4 sections of 30 minutes divided in 2 intervals: “OP MEAN” and “OP MAX” also described in *Figure 9*. During “OP MEAN” interval, the electric motor is fed by the mean current value and its duration is 21 minutes. During “OP MAX”, the electric motor is fed by the maximum current value and its duration is 9 minutes. The 4 sections are combined with two additional time intervals referenced as “Taxi out” and “Taxi in” of 8 minutes and 4 minutes respectively. The architecture is designed to sustain 60000 working cycles.



*Figure 9 Flow and Altitude quantities in working cycle*

## Conduction and switching losses comparison

In order to validate equations (1)-(10), all architectures have been simulated with same boundary conditions. In Table 4 all parameters are summarized where stands for carrier frequency and stands for modulation frequency.

Table Conduction and switching simulation parameters

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  |  |  |  |  |

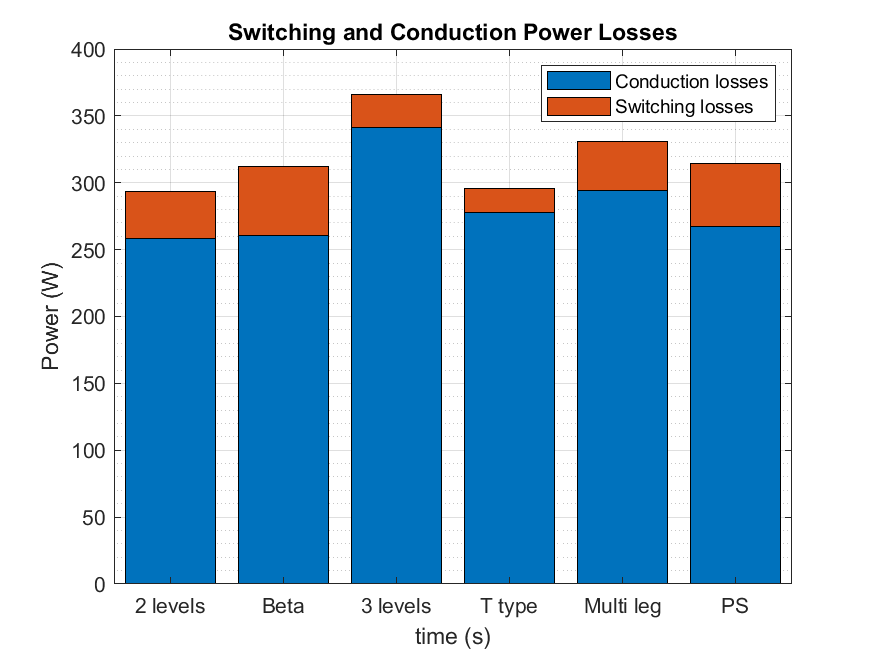


Figure Simulation results for conduction and switching losses

In Figure 10, 3 levels inverter observers the highest amount of losses mainly due to conduction losses contribution. The series of devices and diodes conduction cause high resistance value. Multi leg solution experiences high conduction losses maintaining the lowest number of devices. 2 levels, Beta and Proposed Solution inverters observe same conduction losses contributes. Due to the high number of devices in parallel, T-type solution permits to achieve the lowest switching losses contributes. Conduction losses are comparable with Multi leg.

## Reliability analysis

In order to study the reliability of the architectures, Physics of Failure approach has been used applying the working cycle current values as input signal of the inverter. Acquiring the junction temperature of a single device observing the thermal fluctuation and the mean temperature that affect the durability of devices. Rainflow-counting algorithm reduces complexity of reliability computation.

From plate data, the thermal pulse duration is 7 minutes. As far as the simulations would require too much time and memory resources, the simulated system has been dimensioned with a thermal constant of 0.7 seconds. So the working cycle duration will be 14 seconds. The carrier frequency has been imposed at 20 kHz and 40 kHz for the first and second test respectively. It is worth to underline the dependence of reliability from devices switching speed, i.e. .

From Figure 11 it is possible to observe the junction temperature of a single device during working cycle. 3 levels inverter suffers from the higher temperature values and T-type the lowest ones. It is important to underline that, for each architecture, the most stressed device has been measured.

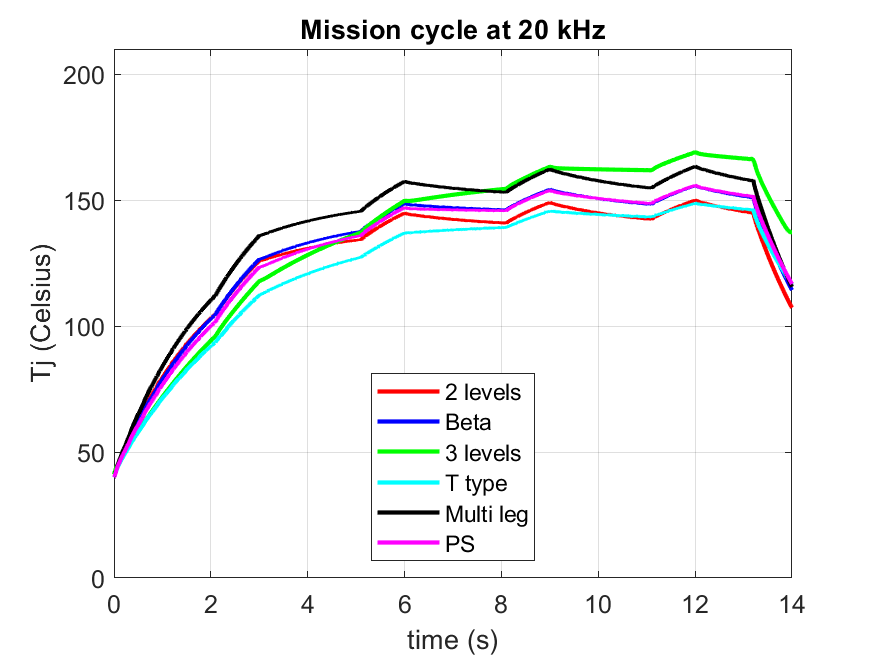


Figure Junction temperature profile for

In Figure 12, as the carrier frequency increases, the junction temperature increases too observing that the most affected. Temperature variation affects reliability with two main phenomena: bond-wire lift off and fatigue due to different coefficient of thermal expansion in the structure of devices.

From Rainflow algorithm, the maximum number of cycles achievable by architectures are listed in Table 5. As expected from temperature profiles, 3 levels observers the lowest reliability properties. It is worth to notice that increasing to 40kHz, only 2 levels, T-type and Proposed solution can match the goal of 60.000 mission cycles.

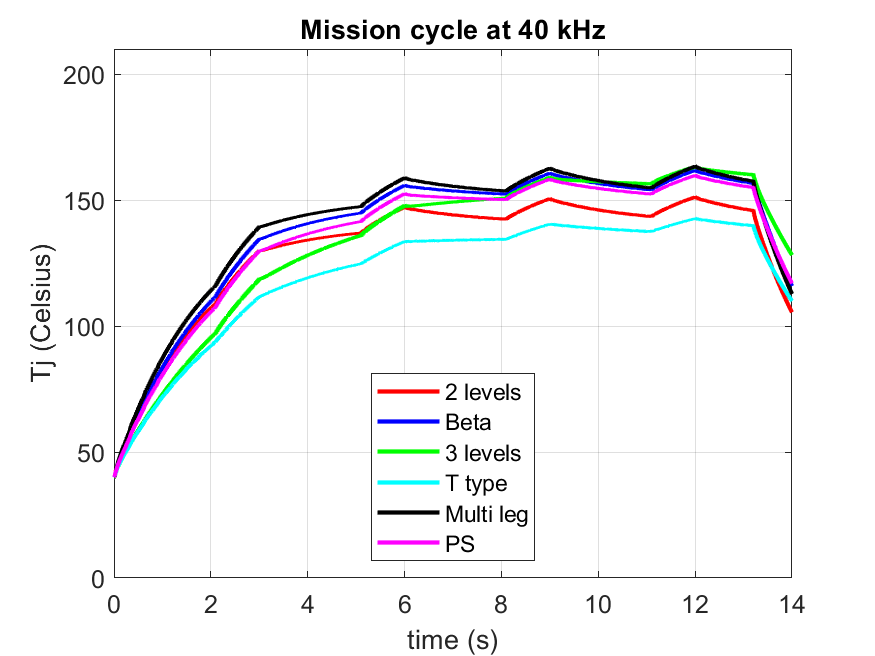


Figure Junction temperature profile for

Table Number of cycles: architectures and carrier frequency

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Architecture | 2 levels | Beta | 3 levels | T-type | Multi leg | PS |
|  | 280786 | 186191 | 84118 | 374436 | 110760 | 184820 |
|  | 93359 | 43167 | 47961 | 221589 | 47693 | 62033 |

## Overshoot analysis model

Overshoot analysis is performed with the combination of 3 models: cable, single coil and motor model. Figure 13 summarizes the overshoot simulation where CCM stands for converter-cable-machine and VD stands for voltage distribution. Basically, lumped element components are exploited to model the elements cable, coils and motor. DM scenario, i.e. differential mode, is studied for overshoot phenomena in phase to phase and phase to ground cases.

Turn to turn overshoot is studied in terms of voltage difference between coils. This phenomenon causes current leakage and power losses in slots that affect the efficiency of the architecture and reliability of electric motor.

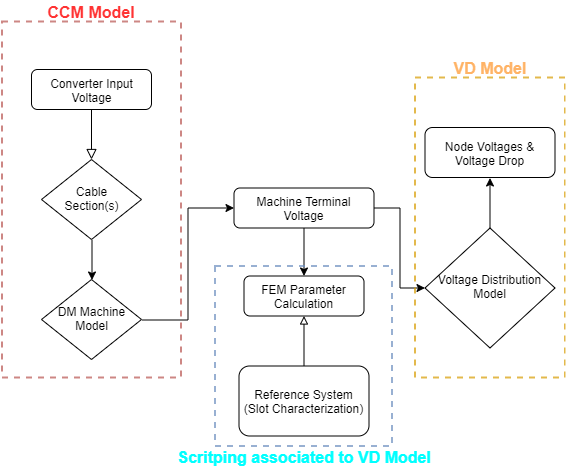


Figure Flowchart of Overshoot simulations model

## Converter induced Voltage Overshoot analysis

As mentioned above, overshoot and non-uniform distributions of the voltage can occur mainly due to the inherently low rise times generated by WBG-based converters. The basic idea is that increasing the number of voltage levels from 0V to VDC should permit to reduce the voltage gradients and thus mitigate the aforementioned challenges. Therefore, different simulations are carried out forcing different rise times of the output voltage waveform. Using the methodology described in Section IV.A, the following quantities are evaluated: 1) phase-to-phase voltage overshoot, 2) phase-to-ground voltage overshoot and 3) turn-to-turn voltages [5]. All values of voltage overshoots are normalized on VDC. The results of Figure 14, Figure 15 and Figure 16 highlight the effectiveness of both the staggered switching and the voltage suppression in the corresponding architectures, i.e. the staggered switching and the multi-leg inverters.

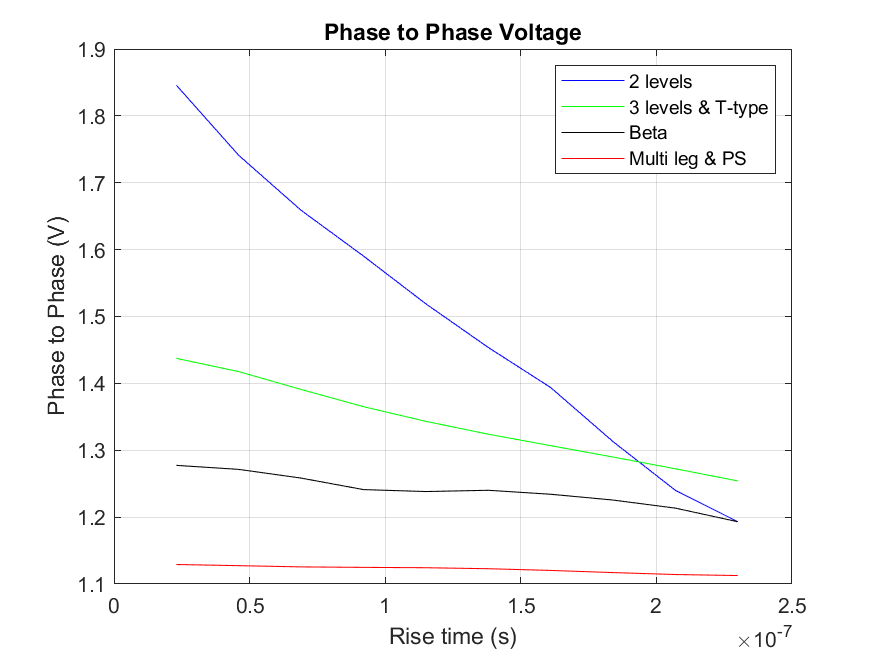


Figure Phase to Phase Voltage overshoot

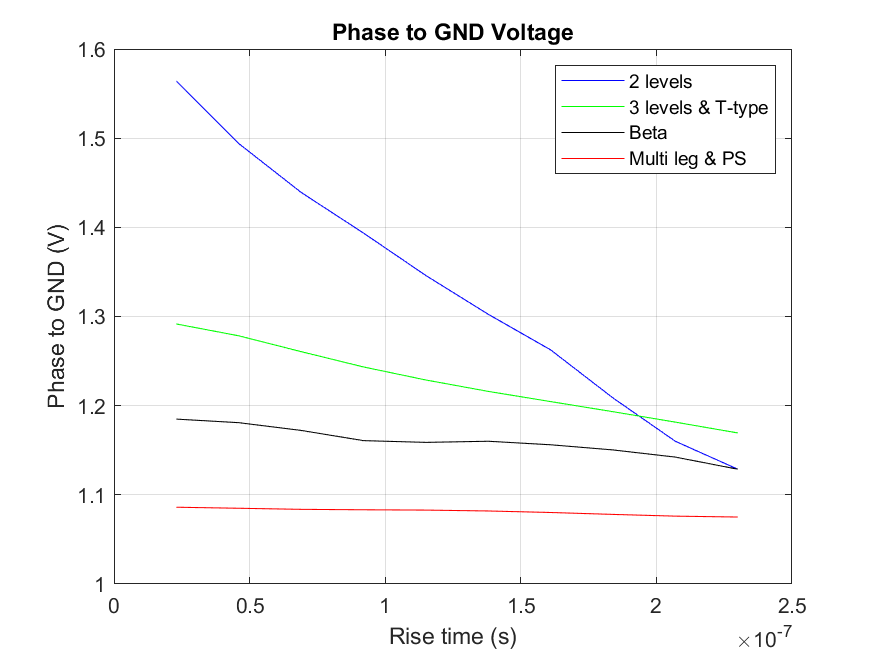


Figure Phase to GND Voltage overshoot

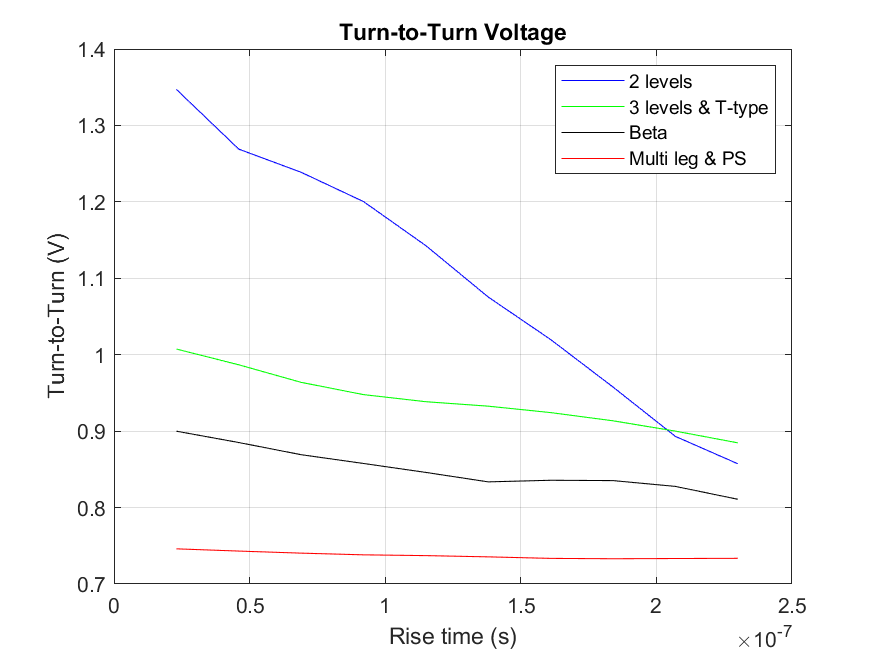


Figure Turn to Turn Voltage overshoot

In particular, at low rise time values, the improvements compared to the worst case scenario represented by the 2 levels inverter is impressive. As rise time increases, all the topologies become comparable in terms of the 3 investigated quantities, yet the last two inverters present an evident benefit.

It should be also noticed that, compared to the 2 level inverter, the T-type, the 3 levels and the β-type inverters achieve good performances in terms of both overshoot and distribution reductions. In particular, the β-type, while not using any specific overvoltage suppression technique, still manages to reduce the unwanted effects.

The conclusion of these analyses is that, although the staggered switching and the proposed multi-leg inverters present better overall performance than the other architectures, their impact on costs and reliability must be carefully evaluated for a more comprehensive investigation. The following sections will therefore deal with such aspects.

Remarking conduction and switching losses, Proposed solution observe lower losses with respect to Multi leg sharing same voltage overshoot behaviour.

# Converter effects on the Electrical Machine

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# Conclusion

The main aim of this research was to prove that active filtering techniques such as the use of suitable inverter architectures can be implemented as a means to mitigate the challenges introduced by WBG semiconductors in electric drive systems. Here, the “suitability” was analysed considering several figures of merit for a number of inverter architectures. First of all, the capability of such inverters to mitigate voltage overshoots at the motor’s terminals and the uneven voltage distribution within the motor’s windings was studied. Then, a detailed power loss analysis was performed both analytically and by means of numerical simulations. Finally, the overall reliability and cost of each of the investigated inverter structures were evaluated. All of the selected inverter solutions were selected using the basic assumption that increasing the number of voltage levels available at the inverter output could improve the abovementioned figures of merit compared to a conventional 2 level architecture used as baseline in this paper.

It was found that 3 levels inverters, named in this work as 3 level, β-type and T-type, improve the voltage overshoots and distributions, while keeping power losses and costs under acceptable limits. However, the reliability was not improved compared to the baseline. The staggered switching inverter showed even more promising results in terms of voltage overshoots and distributions, with the additional benefit of featuring the highest reliability while not compromising the losses. Nevertheless, this solution is by far the most expensive one. Finally, a multi-leg inverter was proposed combining the β-type inverter and the staggered switching technique. This last architecture, compared to the staggered switching solution, showed identical results in terms of voltage overshoots and distributions, a slightly lower reliability and a rather lower overall cost, thus eventually resulting in the most suitable candidate for the sake of this research.

REFERENCE:

1. P. Giangrande, V. Madonna, S. Nuzzo and M. Galea, "Moving Toward a Reliability-Oriented Design Approach of Low-Voltage Electrical Machines by Including Insulation Thermal Aging Considerations," in IEEE Transactions on Transportation Electrification, vol. 6, no. 1, pp. 16-27, March 2020, doi: 10.1109/TTE.2020.2971191.
2. F. Savi et al., "High-Speed Electric Drives: A Step Towards System Design," in IEEE Open Journal of the Industrial Electronics Society, vol. 1, pp. 10-21, 2020, doi: 10.1109/OJIES.2020.2973883.
3. Y. Zhang, Y. Shi and H. Li, "Study of Passive dv/dt Filter and Proposed Active Solution for SiC MV Motor Drive," 2019 IEEE Electric Ship Technologies Symposium (ESTS), Washington, DC, USA, 2019, pp. 236-240, doi: 10.1109/ESTS.2019.8847725.
4. A. Rafiq and R. Maheshwari, "A resonant gate driver circuit with turn-on and turn-off dv/dt control," 2018 IEEMA Engineer Infinite Conference (eTechNxT), New Delhi, 2018, pp. 1-5, doi: 10.1109/ETECHNXT.2018.8385357.
5. D. Barater, J. Arellano-Padilla and C. Gerada, "Incipient Fault Diagnosis in Ultrareliable Electrical Machines," in IEEE Transactions on Industry Applications, vol. 53, no. 3, pp. 2906-29
6. M. Pastura, S. Nuzzo, G. Franceschini, G. Sala, D. Barater, “Sensitivity Analysis on the Voltage Distribution within Windings of Electrical Machines fed by Wide Band Gap Converters”, Proceedings of 2020 XIV International Conference on Electrical Machines (ICEM), Gothenburg, 2020
7. V. Grau and R. W. De Doncker, "The Effects of Steep Voltage Slopes on Insulation Systems of Coil Windings caused by Next Generation Power Semiconductor Devices," 2019 IEEE Electrical Insulation Conference (EIC), Calgary, AB, Canada, 2019, pp. 26-29, doi: 10.1109/EIC43217.2019.9046515.
8. D. R. Meyer, A. Cavallini, L. Lusuardi, D. Barater, G. Pietrini and A. Soldati, "Influence of impulse voltage repetition frequency on RPDIV in partial vacuum," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 25, no. 3, pp. 873-882, June 2018, doi: 10.1109/TDEI.2018.006722.
9. J. He et al., "Multi-Domain Design Optimization of dv/dt Filter for SiC-Based Three-Phase Inverters in High-Frequency Motor-Drive Applications," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5214-5222, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2922306.
10. A. Schroedermeier and D. C. Ludois, "Integration of Inductors, Capacitors, and Damping Into Bus Bars for Silicon Carbide Inverter dv/dt Filters," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 5045-5054, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2920596.
11. M. Pastura, S. Nuzzo, M. Kohler and D. Barater, "Dv/Dt Filtering Techniques for Electric Drives: Review and Challenges," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 7088-7093, doi: 10.1109/IECON.2019.8926663.
12. V. Madonna, P. Giangrande, W. Zhao, H. Zhang, C. Gerada, and M. Galea, “On the design of partial discharge-free low voltage electrical machines,” in2019 IEEE International Electric Machines Drives Conference (IEMDC), pp. 1837–1842, 2019
13. A. Arzillo, P. Braglia, S. Nuzzo, D. Barater, G. Franceschini, "Challenges and Future opportunities of Hairpin Technologies," 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), Delft, Netherlands, 2020, pp. 277-282, doi: 10.1109/ISIE45063.2020.9152417
14. M. S. Islam, I. Husain, A. Ahmed and A. Sathyan, "Asymmetric Bar Winding for High-Speed Traction Electric Machines," in IEEE Transactions on Transportation Electrification, vol. 6, no. 1, pp. 3-15, March 2020
15. P. Nayak and K. Hatua, "Active Gate Driving Technique for a 1200 V SiC MOSFET to Minimize Detrimental Effects of Parasitic Inductance in the Converter Layout," in IEEE Transactions on Industry Applications, vol. 54, no. 2, pp. 1622-1633, March-April 2018, doi: 10.1109/TIA.2017.2780175
16. Y. Jiang, C. Feng, Z. Yang, X. Zhao and H. Li, "A new active gate driver for MOSFET to suppress turn-off spike and oscillation," in Chinese Journal of Electrical Engineering, vol. 4, no. 2, pp. 43-49, June 2018, doi: 10.23919/CJEE.2018.8409349.
17. X. Li et al., "Simple Control Strategies for dv/dt Reduction in SiC MOSFET based Modular Multilevel Converters," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 80-84, doi: 10.1109/WiPDA46397.2019.8998827.
18. E. -S. Jun, M. H. Nguyen and S. -S. Kwak, "Model Predictive Control Method With NP Voltage Balance by Offset Voltage Injection for Three-Phase Three-Level NPC Inverter," in IEEE Access, vol. 8, pp. 172175-172195, 2020, doi: 10.1109/ACCESS.2020.3024634.
19. J. Hong and R. Cao, "Adaptive Selective Harmonic Elimination Model Predictive Control for Three-Level T-Type Inverter," in IEEE Access, vol. 8, pp. 157983-157994, 2020.
20. Sangcheol Lee and Kwanghee Nam, "An overvoltage suppression scheme for AC motor drives using a half DC-link voltage level at each PWM transition," in IEEE Transactions on Industrial Electronics, vol. 49, no. 3, pp. 549-557, June 2002, doi: 10.1109/TIE.2002.1005379.
21. C. Friedrich, T. Fuchslueger, M. Vogelsberger and H. Ertl, "Design Verification of a High-Peak-Current Multi-Leg Sine-Wave Inverter," PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Germany, 2020, pp. 1-7.
22. D. Barater, C. Concari, G. Buticchi, E. Gurpinar, D. De and A. Castellazzi, "Performance Evaluation of a Three-Level ANPC Photovoltaic Grid-Connected Inverter With 650-V SiC Devices and Optimized PWM," in IEEE Transactions on Industry Applications, vol. 52, no. 3, pp. 2475-2485, May-June 2016, doi: 10.1109/TIA.2016.2514344.
23. V. Madonna, P. Giangrande and M. Galea, "Electrical Power Generation in Aircraft: Review, Challenges, and Opportunities," in IEEE Transactions on Transportation Electrification, vol. 4, no. 3, pp. 646-659, Sept. 2018
24. DO-160, Environmental Conditions and Test Procedures for Airborne Equipment, published by RTCA (Radio Technical Commission for Aeronautics).
25. “IAGOS: In-Service Aircraft for a Global Observing System.” https://www.iagos.org/ (accessed Jul. 08, 2020).
26. H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, “Transitioning to physics-of-failure as a reliability driver in power electronics, ”IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 1, pp. 97–114,2014.
27. M. Rausand and A. Høyland, System reliability theory: models, statistical methods, and applications. John Wiley & Sons, 2003.
28. L. Wang, C. Ngai-Man Ho, F. Canales and J. Jatskevich, "High-Frequency Modeling of the Long-Cable-Fed Induction Motor Drive System Using TLM Approach for Predicting Overvoltage Transients," in IEEE Transactions on Power Electronics, vol. 25, no. 10, pp. 2653-2664, Oct. 2010.
29. Scitech Europa,”Ultra lightweight motors for the next electric vehicles”, 25th March 2019
30. J. Rąbkowski and T. Płatek, "Comparison of the power losses in 1700V Si IGBT and SiC MOSFET modules including reverse conduction," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-10, doi: 10.1109/EPE.2015.7309444.
31. D. Oustad, M. Ameziani, D. Lhotellier, S. Lefebvre and M. Petit, "Estimation of the Losses in Si and SiC Power Modules for Automotive Applications," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2017, pp. 1-8.
32. X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang and B. Zhang, "Understanding switching losses in SiC MOSFET: Toward lossless switching," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 257-262, doi: 10.1109/WiPDA.2015.7369295.
33. Yu, Liangchun & Dunne, Greg & Matocha, Kevin & Cheung, Kin & Suehle, John & Sheng, Kuang. (2011). Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments. Device and Materials Reliability, IEEE Transactions on. 10. 418 - 426. 10.1109/TDMR.2010.2077295
34. L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle and K. Sheng, "Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments," in IEEE Transactions on Device and Materials Reliability, vol. 10, no. 4, pp. 418-426, Dec. 2010
35. M. Gurfinkel et al., "Time-Dependent Dielectric Breakdown of 4h-sic/SiO2mos Capacitors," in IEEE Transactions on Device and Materials Reliability, vol. 8, no. 4, pp. 635-641, Dec. 2008.
36. R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 2139-2146, doi: 10.1109/ECCE.2013.6646971.